tor. Also, a lumped element equivalent circuit of the GaAs MESFET chip, which is valid at least up to 12 GHz, was used in the study. (Though some quantitative ambiguity remains to be studied, these assumptions could be accepted as the first approximations.) Fig. 9(c) shows the overall model used for the estimations of the impedance characteristics as a two-terminal device looking from the drain– source port.

B. Impedance Calculation

Fig. 10 shows the calculated impedance characteristics of the model as a function of frequency and with coupling factor "a" as a parameter. The result shows that negative resistance properties can be obtained in the frequency region above the resonance of the feedback structure. As the series resonant circuit, whose resonance is of the order of 20–30 GHz, can be easily realized by properly designing the package lid metallized portion and the FET housing structure, the above result indicates the feasibility of high-gain amplifier in the *Ka*-band.

IV. Conclusion

An experimentally developed reflection-type amplifier using the GaAs MESFET and some discussions using a simplified model have been described. While the quantitative justification of the lumped element approximation assumption used in the simulation model remains to be studied, the results show prospects for realization of a low-noise preamplifier with high gain using the state-of-the-art GaAs MESFET as a negative resistance two-terminal device in *Ka*-band, where conventional three-terminal operation encounters gain degradation problems.

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Performance of a Dual-Gate GaAs MESFET as a Frequency Multiplier at *Ku*-Band

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***Abstract*—The fabrication and characteristics of a dual-gate GaAs MESFET are briefly described. The feasibility of using a dual-gate GaAs MESFET as a novel frequency multiplier over *Ku*-band with good conversion gain is demonstrated. The multiplier achieved 8-dB conversion gain with frequency doubling at 12.6 GHz and 2.5-dB gain with frequency tripling at 12 GHz. In addition, it possessed a built-in control of conversion gain over a 36-dB dynamic range.**

I. Introduction

SINCE the advent of the dual-gate GaAs MESFET in 1971 [1], its applications have been successfully expanded into several areas, such as variable-gain microwave amplifiers [2]–[4], mixers with conversion gain [5], RF power limiters [6], phase-shift-keyed (PSK) modulators at subnanosecond rates [7], and low-noise operations [8]. Compared with its counterpart, the single-gate GaAs MESFET, this FET offers higher small-signal gain, better isolation [3], and inherently more nonlinear characteristics due to the addition of the second gate. Recently, further study concerning its nonlinear behavior has evolved a novel application for frequency multiplication [9].

The purpose of this paper is to demonstrate the feasibility of using a dual-gate GaAs MESFET as a frequency multiplier over *Ku*-band with good conversion gain. In addition, the fabrication and electrical characteristics of such a device are briefly described. Finally, the performance comparison between the single- and dual-gate MESFET multipliers will be discussed.

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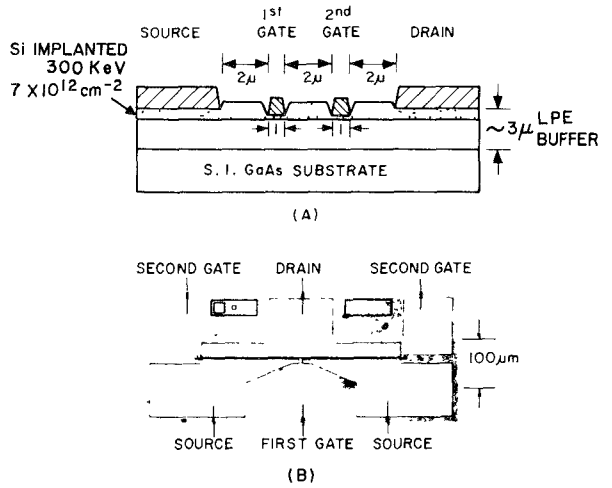


Fig. 1. An ion-implanted dual-gate GaAs MESFET. (a) A schematic cross-sectional view. (b) Microphotography of a complete device.

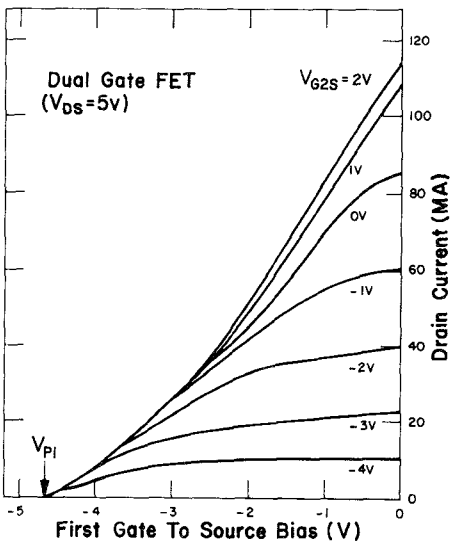


Fig. 2. Typical dual-gate MESFET drain-current characteristics as a function of the bias of both gates, at a drain voltage of 5 V.

II. Device Fabrication

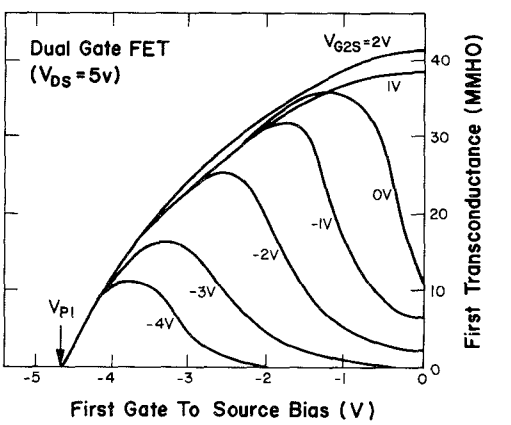
Dual-gate GaAs MESFET's were fabricated on an ion-implanted active layer. The layer was formed by first implanting Si at 300 keV energy, 7×10^{12} cm^{-2} dosage into a high-resistivity buffer layer grown by the liquid-phase epitaxy. Then this layer was annealed at 850° C for 30 min under 0.65-μm SiO_2 encap. The typical measured peak-electron concentration was 1.7×10^{17} cm^{-3}. A cross-sectional view of the device is shown in Fig. 1(a). Both aluminum parallel gates, 2-μm apart, are 1 μm long and 400 μm wide. The gates were aligned in the center of an 8-μm spacing between the source and drain.

All the patterns were defined and aligned photolithographically using AZ positive photoresist. The Al-gate metal was approximately 0.75 μm thick and was deposited by electron beam evaporation. The source and drain ohmic contacts were alloyed Au–Ge [3]. Fig. 1(b) shows the microphotography of a complete dual-gate GaAs MESFET.

III. Device Characteristics

Fig. 2 shows typical dual-gate MESFET drain current characteristics as a function of both gate biases, at a fixed drain voltage. Device first small transconductance g_{m1} is measured between the first gate and drain with the RF-grounded second gate at 1 MHz. This typical characteristic is plotted against the first-gate bias with various second-gate biases in Fig. 3(a). Similarly, Fig. 3(b) shows device second small transconductance g_{m2} versus the second-gate bias, including different first-gate voltages. It is evident that the transfer nonlinearities are readily controllable by either gate bias.

The input characteristic, particularly the second-gate I_{G2}-V_{G2} family is given at $V_{G1S}=0$ V in Fig. 4, where the effect of the drain-to-source voltage is illustrated. The fact that the forward gate turn-on voltage substantially increases with the drain voltage arises partly from a large voltage drop caused by a drain current flowing through the inherently high resistance between the second gate



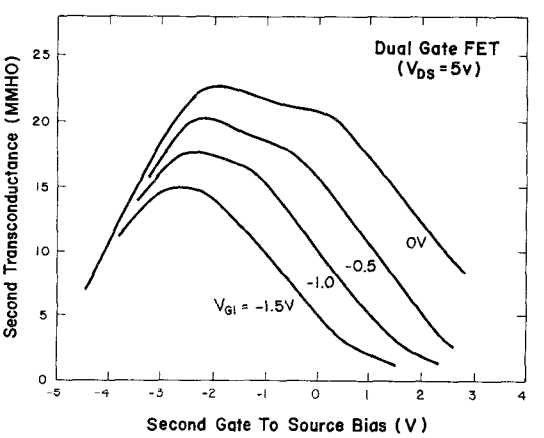


Fig. 3. Dual-gate MESFET small transconductance characteristics. (a) First transconductance g_{m1} versus the first-gate bias with various biases of the RF-grounded second gate. (b) Second transconductance g_{m2} versus the second-gate bias with various biases of the RF-grounded first gate.

and source. Also, the gate current flows towards the drain at higher gate biases. It will be discussed later that this unique feature plays an important role in frequency multiplication.

Measured in the common-source mode at 10 GHz, the device exhibits the following major results: 12.5-dB maxi-

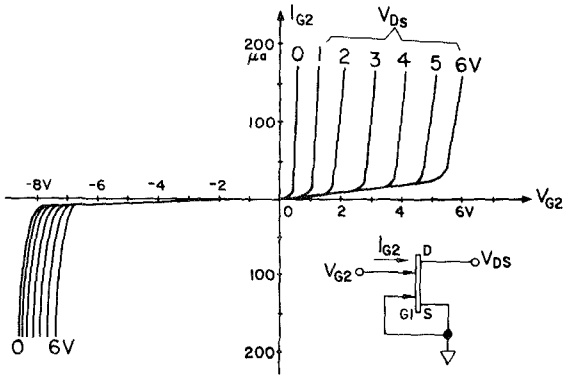


Fig. 4. Second gate input characteristics of a dual-gate MESFET with variations of the drain-to-source voltage. The first gate is dc-grounded.

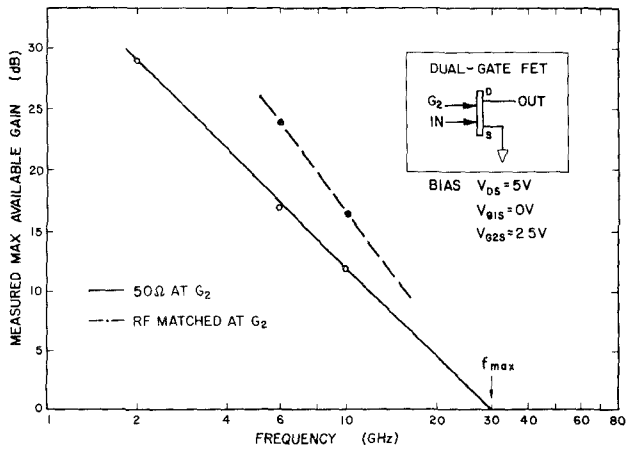


Fig. 5. Measured maximum available gain versus frequency, at a small-signal condition, with two different loads presented at the second gate.

mum available gain under small-signal conditions, with the second gate terminated with 50-Ω and 16-dB gain with the same gate RF-matched. The extrapolated f_{max} is around 30 GHz as shown in Fig. 5. In addition, a gain control of over 45 dB at 10 GHz is easily achieved by adjusting the second-gate voltage. In terms of power performance, this device is capable of delivering 18 dBm with an associated gain of 11 dB.

IV. Multiplier Test Arrangement

In general, a single-gate GaAs MESFET has two kinds of nonlinearities: one is the drain-current/gate-voltage transfer nonlinearity, and the other is the gate-voltage/current-input nonlinearity. The use of either one can be well suited for frequency conversion. Utilizing both nonlinearities in a dual-gate MESFET can also result in frequency multiplication. To understand the principle of operation consider the illustration in Fig. 6. A dual-gate MESFET can be adequately modeled as two single-gate MESFET's connected in cascade [3]; the first MESFET is operated with a common source, yet its drain current feeds the source of the second MESFET. Initially, the first-gate transconductance is periodically modulated by an input signal. The amplified signal swing at the source

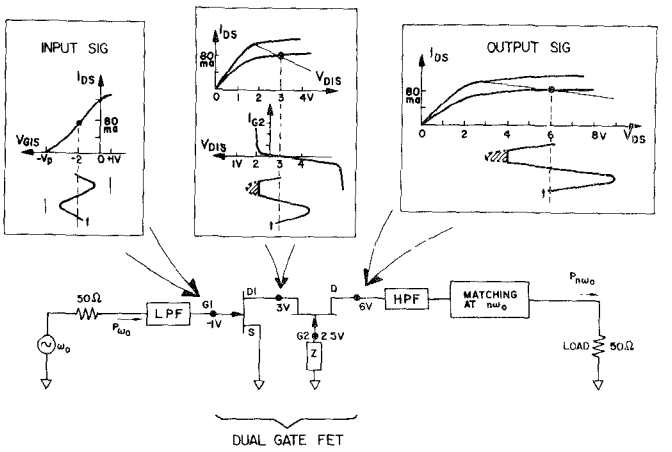


Fig. 6. Basic operating principles of frequency multiplication in a dual-gate MESFET.

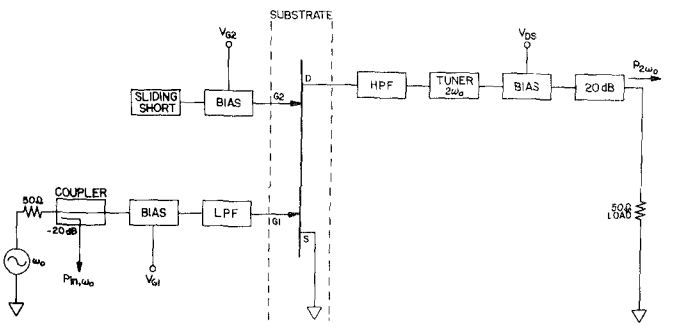


Fig. 7. Dual-gate MESFET doubler test circuit arrangement. For ease of testing, no tuner at the first gate is used.

of the second MESFET is, in turn, clipped by its input nonlinearity previously alluded to in Fig. 4, thereby generating harmonics. The resultant harmonics are further amplified and extracted from the second MESFET drain. The clipped drain-voltage waveform controlled by the bias of both gates essentially dictates the harmonic content.

A simple test circuit arrangement for measuring frequency doubling at *Ku*-band is depicted in Fig. 7. An input frequency ω_0, ranging from 6 to 9 GHz, is applied to the first gate through a 9.2-GHz low-pass filter, while a tuner is placed at the drain for maximizing the output power at the doubling frequency $2\omega_0$. However, for ease of testing, the use of a tuner at the first gate is avoided. Instead, the first gate is shunted with a 50-Ω load. It is essential to extract the output frequency through a high-pass filter, thus suppressing the input frequency. Because the purely reactive fundamental match to the second gate is quite important for the gain [3], a sliding short is used at the second gate to enhance conversion efficiency. The doubler conversion efficiency $\eta_{2\omega_0}$ usually expressed in decibels is given as

$$\eta_{2\omega_0}(\text{dB}) = P_{\text{out},2\omega_0}(\text{dBm}) - P_{\text{in},\omega_0}(\text{dBm}) \qquad (1)$$

where $P_{\text{out},2\omega_0}$ is an output power in dBm extracted at the doubling frequency $2\omega_0$, and P_{in,ω_0} is an input power in dBm at the fundamental frequency ω_0.

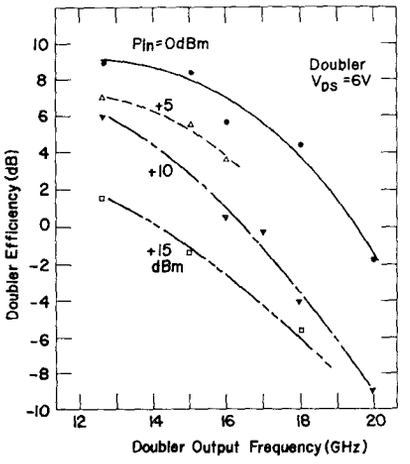


Fig. 8. Dual-gate MESFET doubler conversion efficiency versus output frequency. Device bias is adjusted at each data point.

V. Experimental Results

The dual-gate MESFET is normally operated in the common-source mode. For frequency doubling, Fig. 8 shows the measured conversion efficiency versus the output frequency from 12 to 18 GHz. The input power dependence is also given. With a drain bias of 6 V both gate biases were adjusted at each data point for the maximum doubler efficiency. At 0-dBm input power, a conversion gain of 8 dB was measured at 12.6 GHz and 4-dB gain at 18 GHz.

As input power increases, the first gate gradually reaches a forward bias condition, thereby reducing the average drain current due to a self-bias phenomenon. Hence, the large decrease in the drain average current caused simultaneously by the self-bias effect of both gates is primarily responsible for the observed doubler efficiency decline with increasing input power. Ultimately, the efficiency is restricted by the device power-handling capability.

For the sake of comparison, a frequency doubler employing a 1-μm single-gate MESFET with 500-μm gate width was tested. Its best conversion efficiency at 12.6 GHz was at least 4 dB lower than the dual-gate results shown in Fig. 8. Clearly, the dual-gate MESFET manifests its superiority as far as nonlinearity is concerned. Compared with a bipolar transistor multiplier [10] and a varactor multiplier [11], the dual-gate MESFET multiplier exhibits better efficiency.

An attempt was also made to explore the feasibility of frequency tripling using a test arrangement similar to that in Fig. 6. In this case, the tripler conversion efficiency expressed in decibels is defined as

$$\eta_{3\omega_0}(\text{dB}) = P_{\text{out},3\omega_0}(\text{dBm}) - P_{\text{in},\omega_0}(\text{dBm}) \qquad (2)$$

where $P_{\text{out},3\omega_0}$ is the output power in dBm extracted at the tripling frequency $3\omega_0$. In Fig. 9, the measured tripler conversion efficiency with different input powers is plotted against the output frequency from 12 to 18 GHz. At 0-dBm input power, the observed conversion gain is 2.5 dB at 12 GHz, and -2 dB at 18 GHz. Again, the

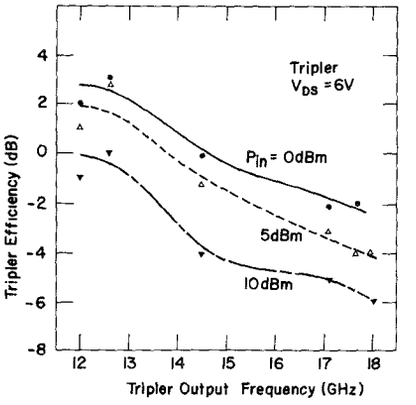


Fig. 9. Dual-gate MESFET tripler conversion efficiency versus output frequency. Device bias is adjusted at each data point.

underlying mechanisms responsible for the tripler efficiency falloff with input power are similar to those previously discussed for the doubler.

Convenient bias control by the second gate allows the dual-gate MESFET frequency multiplier to vary its conversion efficiency. It was possible to vary this efficiency over a range of 36 dB at 12.6 GHz. Since this device is known to show four characteristic operating modes depending on its bias conditions [8], the measured variation of the efficiency is not monotonic with the second-gate voltage.

VI. Conclusions

Given the pronounced transfer nonlinearity controllable by either gate bias, the dual-gate GaAs MESFET has demonstrated feasibility for generating frequency multiplication with good conversion gain at *Ku*-band. The experimental multiplier benefits from a built-in variable conversion gain control. It is worth noting that the observed conversion gain can be further improved through impedance matching at the input gate. In comparison, the dual-gate MESFET multiplier offers the advantages of better efficiency and easier gain control over its single-gate MESFET counterpart [12].

Finally, the practicality of the dual-gate MESFET promises future potential for even higher frequency applications (beyond 18 GHz) which will undoubtedly complement the rapidly improving *K*-band GaAs MESFET's [13].

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Silicon Bipolar Microwave Power Transistors

RICHARD ALLISON

Invited Paper

***Abstract*—This paper presents a review of the present status of commercially available silicon bipolar transistors and projects what power at frequency performance will be available in the next few years. It discusses the need for implementing certain fabrication/processing developments necessary to meet the projected power at frequency performance levels.**

I. Introduction

THIS ARTICLE is in the form of a review discussing the present status of commercially available silicon bipolar transistors relative to GaAs FET R&D developments. The article also projects what power at frequency performance will be available in the next few years. It discusses the need for implementing certain fabrication/processing developments necessary to meet the projected power at frequency performance levels.

It is interesting to contemplate the data summarized in Fig. 1. First, it is clear that the data fit a $Pf^2 = \text{constant}$ equation (where P = power-out, and f = frequency). Second, both GaAs FET's and Si bipolar transistors' pulse data fit a single line. The implication is that, from a peak power capability standpoint, there is little difference in performance between silicon bipolar and GaAs FET's at the present state of their development, probably because the present FET structures are not optimized to take advantage of the inherently superior GaAs properties. Third, the CW capabilities of silicon bipolars are lower than their pulse power levels by a factor of about 1.8, because the operating junction temperature is lower for pulsed operation than for CW at fixed power and efficiency. This is due to the reduced thermal interference between adjacent transistor cells whenever the pulse period is less than the transistor thermal time constant. Effectively, Θ_{jc} is improved under pulsed conditions, allowing higher power to be attained. The comparison here cannot be exact between GaAs FET's and silicon bipolars because they are not in a common package configuration. However, there is definitely the need for the thermal resistance Θ_{jc} of Si bipolars to be reduced in order to raise their CW power capabilities to the levels achieved under pulse conditions.

Since one can sacrifice gain in order to gain power, the discussion of Fig. 1 would not be complete without reference to Table I where the data used in the Pf^2 plot are shown indicating the gains and the power added efficiencies associated with those power levels. Unlike silicon bipolar devices, the GaAs FET's can be driven to higher power by allowing gain compression, and the data in Table I are in effect power-out levels achieved under drive conditions such as to maintain gains to about 4-dB levels.

In comparison to silicon bipolar transistors, the higher scatter-limited velocity and the absence of minority carriers in GaAs FET's have made GaAs FET's applicable for high-frequency operation. However, developments in bipolar technology are in progress that will substantially increase the frequency capability by increasing both

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